SPECIFICATION AMENDMENTS

Please replace paragraph 0019 with the following rewritten paragraph:

0019 For example, the gate dielectric layer 14B deposition may take place at a temperature of from about 250 °C to about 1050 °C and may include oxidation or nitridation processes following deposition as well as one or more post deposition annealing process, including furnace or RTA annealing. It will be appreciated that the post deposition annealing processes may be carried out following subsequent buffer layer or gate electrode material deposition and/or gate structure formation as explained below. The post deposition annealing processes may include temperatures from about 300 °C to about 1100 °C. The post deposition annealing processes may be carried out in [[an]] inert gas, hydrogen, nitrogen, oxygen, or mixtures thereof.

Please replace paragraph 0020 with the following rewritten paragraph:

0020 It will be appreciated that the thickness of the high-K gate dielectric layer 14B will vary depending on the equivalent oxide thickness (EOT) desired, for example and EOT of between about 5 Angstroms and 50 Angstroms. For example, the gate dielectric layer may vary between about 40 Angstroms and about 100 Angstroms.

Please replace paragraph 0022 with the following rewritten paragraph:

0022 In one embodiment, the buffer layer 16 is formed of a non-metal containing dielectric selected from the group consisting of semiconductor-oxide, semiconductor-nitride, oxides, nitrides, silicates and semiconductor-silicates. For example, the buffer layer 16 is doped with nitrogen to form silicon nitrides, silicon oxynitrides, silicate nitrides, and silicate oxynitrides. For example, the buffer layer may be formed of silicon nitride (e.g., Si_xN_y) or silicon oxynitride (e.g., $Si_xO_yN_z$) or combinations thereof including a dopant

gradient having a dopant concentration ~~increasing~~ decreasing from a bottom portion of the buffer layer to an upper portion. For example, the buffer layer is gradiently doped to form a higher dielectric constant at a bottom portion and a lower dielectric constant at an upper portion, but preferably having an overall dielectric constant greater than about 3.9.

Please replace paragraph 0026 with the following rewritten paragraph:

0026 The metal dopant may be uniformly doped throughout the buffer layer or may be gradiently doped. For example, a metal doped silicate nitride such as $HfSi_xO_yN_z$ for an NMOS device and $AlSi_xO_yN_z$ for a PMOS device is preferably included in the buffer layer having a metal doping at less than about 40 atomic percent with respect to silicon, more preferably less than about 20 atomic percent. Preferably, the same or different metal dopant ~~as is~~ included in the high-K gate dielectric layer 14B is included in the buffer layer at a lower concentration. For example one or more of Hf, Al, Ti, Ta, Zr, La, Ce, Bi, W, Y, Ba,

Sr, and Pb may be included as a metal dopant in the buffer layer, for example forming a material such as MO_xN_y, MSi_xO_y, MSi_xN_y, $MxSiO_yN_z$, where M is a metal dopant. Preferably, the buffer layer has a dielectric constant greater than about 3.9. In forming a gradiently doped buffer layer the direction of metal dopant concentration gradient is preferably from a higher metal dopant concentration at the bottom portion of the buffer layer (high-K dielectric layer/buffer layer interface) to a lower metal dopant concentration in the uppermost portion (buffer layer/gate electrode interface).

Please replace paragraph 0027 with the following rewritten paragraph:

0027 Referring to Figure 1D, following formation of the buffer layer 16, a gate electrode material layer 18 is formed over (on) the buffer layer 16, for example having a thickness less than about 2500 Angstroms. The gate electrode material may include polysilicon, amorphous polysilicon, polysilicon-germanium, metals, metal silicides, metal nitrides, metal

oxides, or combinations thereof. Preferably, the gate electrode material at the gate electrode/buffer layer interface is a semiconductor material having a forbidden energy band gap (E_g). For example, the portion of the gate electrode at the buffer layer/gate electrode interface [[is]] preferably includes a semiconductor material such as polysilicon, amorphous polysilicon, and polysilicon-germanium. The gate electrode layer 18 may be deposited by CVD, LPCVD, ALD-CVD, PECVD, or PVD methods as are known in the art.